What is claimed is:

~~1. An SRAM memory cell comprising:~~

first and second transfer gate transistors, the first transfer gate transistor having a first source/drain connected to a bit line and the second transfer gate transistor having a first source/drain connected to a complement bit line and each transfer gate transistor having a gate connected to a word line; and

first and second pull-down transistors configured as a storage latch, the first pull-down transistor having a first source/drain connected to a second source/drain of said first transfer gate transistor and the second pull-down transistor having a first source/drain connected to a second source/drain of said second transfer gate transistor, both first and second pull-down transistors having a second source/drain connected to a power supply voltage node;

wherein the first and second transfer gate transistors each include a gate oxide layer having a first thickness, the first and second pull-down transistors each include a gate oxide layer having a second thickness, and the first thickness is different from the second thickness.

2. The SRAM memory cell of claim 1, wherein the first thickness is thicker than the second thickness.

3. The SRAM memory cell of claim 2, wherein the first thickness is greater than two times the second thickness.

4. The SRAM memory cell of claim 1, wherein the first and second thicknesses are determined as follows:

$$RATIO \leq \frac{Tox_{tg}}{Tox_{pd}} \frac{W_{pd}/L_{pd}}{W_{tg}/L_{tg}} \frac{Vcc-Vt_{tg}}{Vcc-Vt_{pd}}$$

where RATIO is the desired ratio of the transfer gate transistors and the pull-down transistors, Tox_{tg} is the gate oxide thickness of the transfer gate transistor, Tox_{pd} is the gate oxide thickness of the pull-down transistor, W_{pd} is width of the pull-down transistor, L_{pd} is the length of the pull-down transistor, W_{tg} is the width of the transfer gate transistor, L_{tg} is the length of the transfer gate transistor, Vt_{tg} is the threshold voltage of the transfer gate transistor, and Vt_{pd} is the threshold voltage of the pull-down transistor.

5. The SRAM memory cell of claim 4, wherein RATIO is equal to 2.6.

6. A method for fabricating two transistors in a semiconductor device comprising:

forming a first transistor having a first gate including a gate oxide layer having a first thickness; and

forming a second transistor having a second gate including a gate oxide layer having a second thickness, wherein the second thickness is greater than the first thickness.

7. The method of claim 6, wherein said step of forming a second transistor comprises:

forming a gate oxide over a substrate in a region of the second transistor when the first gate is formed, wherein the gate oxide layer in region of the second transistor initially has a first thickness;

thereafter, depositing a protective layer over the semiconductor device;

opening a window in the protective layer over the region of the second transistor;

etching away the gate oxide in the window to expose the substrate; and

13. A semiconductor circuit comprising:

a first transistor having a first gate including a gate oxide layer having a first thickness; and

a second transistor having a second gate including a gate oxide layer having a second thickness, wherein the second thickness is greater than the first thickness.

14. The semiconductor circuit of claim 13, wherein the first transistor is a pull-down transistor in an SRAM memory cell.

15. The semiconductor circuit of claim 14, wherein the second transistor is a transfer gate transistor in the SRAM memory cell.

16. The semiconductor circuit of claim 15, wherein the gate oxide thickness of the pull-down transistor and a transfer gate transistor in the SRAM memory cell are selected using the following:

$$RATIO \leq \frac{Tox_{tg}}{Tox_{pd}} \frac{W_{pd}/L_{pd}}{W_{tg}/L_{tg}} \frac{Vcc-Vt_{tg}}{Vcc-Vt_{pd}}$$

where RATIO is the desired ratio of the transfer gate transistors and the pull-down transistors, Tox_{tg} is the gate oxide thickness of the transfer gate transistor, Tox_{pd} is the gate oxide thickness of the pull-down transistor, W_{pd} is width of the pull-down transistor, L_{pd} is the length of the pull-down transistor, W_{tg} is the width of the transfer gate transistor, L_{tg} is the length of the transfer gate transistor, Vt_{tg} is the threshold voltage of the transfer gate transistor, and Vt_{pd} is the threshold voltage of the pull-down transistor.

17. The semiconductor circuit of claim 16, wherein RATIO is at least 2.6.

18. The semiconductor circuit of claim 11, wherein the pull-down transistor is an n-channel field effect devices.

19. The semiconductor circuit of claim 10, wherein the transfer gate transistor is an n-channel field effect device.

forming a gate oxide on the exposed substrate until a gate oxide layer of the second thickness is reached.

8. The method of claim 7, wherein said step of forming a second transistor comprises:

forming a gate oxide layer over a substrate in a region of the second transistor when the first gate is formed, wherein the gate oxide layer in the second gate has a thickness equal to the first thickness; and

forming additional gate oxide on the gate oxide layer in the region of the second transistor until the gate oxide layer in the region of the second transistor reaches the second thickness.

9. The method of claim 4, wherein the step of forming a first transistor comprises forming a pull-down transistor in an SRAM memory cell.

10. The method of claim 9, wherein the step of forming a second transistor comprises forming a transfer gate transistor in the SRAM memory cell.

11. The method of claim 10, wherein the steps of forming a pull-down transistor and a transfer gate transistor in the SRAM memory cell comprises forming the transistors to achieve a resistivity ratio as follows:

$$RATIO \leq \frac{Tox_{tg}}{Tox_{pd}} \frac{W_{pd}/L_{pd}}{W_{tg}/L_{tg}} \frac{Vcc-Vt_{tg}}{Vcc-Vt_{pd}}$$

where RATIO is the desired ratio of the transfer gate transistors and the pull-down transistors, Tox_{tg} is the gate oxide thickness of the transfer gate transistor, Tox_{pd} is the gate oxide thickness of the pull-down transistor, W_{pd} is width of the pull-down transistor, L_{pd} is the length of the pull-down transistor, W_{tg} is the width of the transfer gate transistor, L_{tg} is the length of the transfer gate transistor, Vt_{tg} is the threshold voltage of the transfer

gate transistor, and Vt_{pd} is the threshold voltage of the pull-down transistor.

12. The method of claim 11, wherein the step of forming the transistors includes using a RATIO equal to at least 2.6.